Network Processors
Evolution and Current Trends
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Network Processors: Evolution & Trends

- Overview of Network Processing
- Drivers & Demands for Network Processing
- What is a “Network Processor”? 
- Characteristics of Network Processors
- Few Examples & Trends

- Acknowledgements: Primary source of the material is www….
  - Pretty pictures are courtesy of RMI’s marketing team
Enterprise Network

Internet Access  Firewall/Routing  Caching & Load-Balancing  Access  Application  Database

Internet And/Or Intranet

Router/Firewall

Internet Access

Web Servers  Application

Storage

Individual Information

Customer Internet

And/Or Intranet
Mobile Communication and Information Convergence

3G Interfaces
- **Uu** – Between Node B and User Equipment
- **lub** – Between Node B and RNC
- **lur** – Between RNC
- **lur-g** – Between BSC and RNC
- **lur-CS** – Between RNC and Circuit Switched Core Network
- **lur-PS** – Between RNC and Packet Switched Core Network
- **Gb** – Between Node B and BTS
- **Abis** – Between BSC and RNC
- **Uu** – Between Node B and User Equipment
- **Um** – Between BTS and UE
- **UTRAN** – Universal Terrestrial Radio Access Network (3G)
- **GERAN** – GSM Edge Radio Access Network (2G/2.5G)
- **BTS** – Base Transceiver Station (Base Station in 2G)
- **Node B** – Base Station in 3G
- **RNC** – Radio Network Controller (3G)
- **BSC** – Base Station Controller (2G/2.5G)
- **SGSN** – Serving GPRS Support Node
- **GGSN** – Gateway GPRS Support Node
- **MGW** – Circuit Switched Media Gateway
- **MSC** – Mobile Switching Center
- **PSTN** – Public Switched Telephone Network
- **PS** – Packet Switch
- **IP** – Internet Protocol

**Note** – MSC and MGW have one to many relationship
Service Delivery Networks

"Bit Shuffling"

"Information Shuffling"

WIRED

Traffic Management
Application Awareness
Deep Packet Inspection
Security

WIRELESS
Traffic Growth

User Traffic
2x / 12 months

Trends
Network Traffic
(2x / 12 Months)
Compute Capacity
(2x / 18 Months)

Source: Prorating Data from Nick McKeown (Stanford University)
• Consumer and Service provider demand, as well as increase in available bandwidth, are driving data traffic growth in the infrastructure

• Processors need to evolve to meet the needs of content traffic growth in the Emerging Infrastructure
Today’s Networks

- Continuously growing traffic
- Higher rates
- Rich set of features
  - Security
    - VPN/IPSec, SSL, Firewalls
  - Application Awareness
  - Deep Packet Inspection
  - Traffic Engineering – QoS/SLA etc.

More processing/inspection/decision making needed at much higher rates
Early “Network Processors”

- Interface Message Processor (IMP)
  - Connected Computers to ARPANET

- Honeywell DDP-516 minicomputer

Wikipedia: Leonard Kleinrock and the first IMP. Taken from [http://www.lk.cs.ucla.edu/personal_history.html](http://www.lk.cs.ucla.edu/personal_history.html)
### Processing Requirements

**Control Plane Requirements**
- High performance
- High I/O bandwidth
- Large memory capacity
- Low-latency memory access
- Power performance

**Data Plane Requirements**
- Low latency/low packet loss/high throughput
- High performance packet processing
- High I/O bandwidth
- Variety of high-speed I/O interfaces
- Low latency/high bandwidth memory access
Processing Elements used in Networking

• **General Purpose Processors**
  – Control Plane Applications
  – Dataplane (albeit, “lower” performance) applications
  – Examples
    • X86 – Intel, AMD
    • PowerPC – FreeScale, AMCC
    • MIPS, ARM – Various Vendors

• **General Purpose Processor + Co-Processor**

• **ASICs**
  – Forwarding, Policing, Shaping, QoS/Traffic Management……

• **Single/Multi-Core System-on-a-chip (SOC)**
  – Traditionally referred to as Network Processor
Motivation for Multiple Cores

- A new 64-byte packets arrives every 64ns on a 10G port
  - Including IPG and Preamble

- With zero overhead for packet reception and transmission functions, a 1Ghz processor provides a 64 cycle budget

<table>
<thead>
<tr>
<th>Processor(Ghz)</th>
<th>Cycles</th>
<th>Inst/Cycle (IPC)</th>
<th>Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>192</td>
<td>0.75</td>
<td>144</td>
</tr>
<tr>
<td>3</td>
<td>192</td>
<td>1.25</td>
<td>240</td>
</tr>
<tr>
<td>5</td>
<td>320</td>
<td>0.75</td>
<td>240</td>
</tr>
<tr>
<td>5</td>
<td>320</td>
<td>1.25</td>
<td>400</td>
</tr>
<tr>
<td>10</td>
<td>640</td>
<td>0.75</td>
<td>480</td>
</tr>
<tr>
<td>10</td>
<td>640</td>
<td>1.25</td>
<td>800</td>
</tr>
</tbody>
</table>
Motivation for Multiple Cores

- IPC (Instructions/Cycle) is affected by memory subsystem performance
  - DRAM latency does not scale as the processor frequency
  - Cycles are wasted waiting for memory
    - % loss is higher at higher clock frequencies

\[\text{Trends}\]

- Network Traffic
  - 2x / 12 Months
- Compute Capacity
  - 2x / 18 Months
- DRAM Access Time
  - 1.1x / 18 Months

Source: Prorating Data from Nick McKeown (Stanford University)
Frequency is not the answer

- A theoretical 10Ghz processor with a “reasonable” IPC provides an instruction budget in 100s of instructions
- Not sufficient for today’s packet processing functions
- Higher Frequency of Operation for CPU will result in “hot” CPUs
- System Power constraints alone prevent pushing the operating frequency
Multiple Cores/Processing Elements

• Packet Processing lends itself very well to parallel processing
  – Work on multiple packets/flows simultaneously

• N processing elements increase the cycle budget by factor of N
  – Referring to earlier 10G, 64-byte packet example:
    • 1 CPU = 64ns budget
    • 2 CPU = 128ns budget
    • 8 CPU = 512ns budget
      – Not accounting for other overheads

• Pipelining of functions achieves similar results
Multi-threading Improves Throughput

• Networking Applications benefit significantly from multi-threaded architectures
  – Memory latencies are more effectively hidden
  – Cache-miss penalties are reduced or eliminated
  – Branch mis-predict penalties avoided

• Better computation density and power performance ratio
Network Processor Attributes

• Number of Cores and/or Processing Elements
  – Homogenous vs. Heterogenous Resources
• Hardware Accelerators and “off-load” capabilities
• Types of Interfaces
  – Memory, 1G, 10G, SPI, PCI, HT etc.
• Programmability
  – General Purpose Programming
  – Changing Standards
  – New Features
  – Bug Fixes
• Ease of programming
  – Very critical for adoption
  – Code Maintenance
Few Examples
Intel – IXP2800

Source: Microprocessor Report
IXP - MicroEngine

Source: Microprocessor Report
IBM - PowerNP

AMCC – nP3700

Source: AMCC Website
Agere PayloadPlus

- FPP = Fast Pattern Processor
- RSP = Routing Switch Processor

Source: Hot Chips 2001
Motorola - C5

Source: Motorola Website
EZChip – NP1/2

TOP = Task Optimized Processor

<table>
<thead>
<tr>
<th>Function</th>
<th>Type of TOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet parse</td>
<td>TOPparse</td>
</tr>
<tr>
<td>Lookup and classify</td>
<td>TOPsearch</td>
</tr>
<tr>
<td>Forwarding and QoS</td>
<td>TOPresolve</td>
</tr>
<tr>
<td>decisions</td>
<td></td>
</tr>
<tr>
<td>Packet modify</td>
<td>TOPmodify</td>
</tr>
</tbody>
</table>

Source: EZchip Website
Cisco - Toaster 3

Source: Microprocessor Report
Toaster TMC

Figure 2. Each TMC within a cluster has its own instruction memory; each pair shares data memory, control registers, and a memory-management unit.

Source: Microprocessor Report

Figure 3. A typical Toaster3 system shown by Cisco in its MPF presentation contains four T3 chips connected in a serial multiprocessing configuration to perform packet forwarding for several line cards with an aggregate throughput up to 10Gb/s.
Xelerated – Xelerator X10q

Source: Microprocessor Report
Bay MicroSystem - Chesapeake

Source: CommDesign
Broadcom - 1250

Source: Microprocessor Report
FreeScale - 8641D

Note: The MPC8641, a pin-for-pin compatible, single-core implementation of the dual-core device is also available. This device offers the same level of bus and interface integration, but it includes only one e600 core built on Power Architecture™ technology.

Source: FreeScale Website
PA Semi - PWRficient PA6T-1682M

Source: Microprocessor Report
Broadcom - 1480

Source: Broadcom Website
Multiple BRCM 1400 Connectivity

Source: Microprocessor Report
Cavium – Octeon Plus

OCTEON Plus CN58XX - Block Diagram

Source: Cavium Network’s website
RMI - XLR

• Up to 8 MIPS64™ XLRTM Cores
  – Up to 1.2GHz Operation
  – 32 Fine Grain Threads
  – 32KB/32KB L1 DedicatedPlusTM cache
  – Unaligned memory access acceleration
  – 8-banked 2MB L2 Cache, 8 trans/clk
  – Fully cache-coherent design

• Full speed Interconnects
  – Fast Messaging Network
  – Memory Distributed Interconnect
  – I/O Distributed Interconnect

• Quad 800MHz DDR2 Controllers

• Autonomous Security Engines
  – Quad Parallel CryptoCores
  – 10Gbps Bulk Encryption + RSA
  – Single pass multi-operations
  – DES/3DES/AES/GCM/ARC4, Kasumi f8
  – SHA-1/256/384/512, MD5, Kasumi f9

• Dual 10Gbps Ports
  – SPI-4.2 and Native 10GE interfaces
  – SPI-4.2 Pass-Through

• Quad 1GE Ports
• Native Hypertransport Port
• Native QDRSRAM/LA-1 Port
SUN - Niagara 2

- 8 SPARC Cores, 4MB shared L2 cache
- 64-bit SPARC V9 instruction set
- Each SPC has the following features:
  - Supports concurrent execution of 8 threads
  - 1 load/store, 2 Integer execution units
  - 1 Floating point and Graphics unit
  - 8-way, 16 KB I$; 32 Byte line size
  - 4-way, 8 KB D$; 16 Byte line size
  - 64-entry fully associative ITLB
  - 128-entry fully associative DTLB
  - MMU supports 8K, 64K, 4M, 256M page sizes; Hardware Table walk
  - Advanced Cryptographic unit
  - Two 10G Ethernet (XAUI) ports on chip
  - Cryptographic coprocessor – 1 per Core
  - On-chip PCI-Express, Ethernet, and FBDIMM memory interfaces are SerDes based
Tilera – TILE64

Source: Microprocessor Report
FreeScale – MultiCore SOC Roadmap

Source: Microprocessor Report
Differentiating NP Attributes

- **Processing Elements**
  - Special/Fixed function
  - General Purpose CPUs
  - Multi-threading

- **Instruction Set**
  - Custom
  - General Purpose
    - MIPS, PowerPC
    - RISC, VLIW

- **Memory Subsystem**
  - Bus, Ring, Mesh
  - Coherent
  - Buffer forwarding

- **Acceleration Functions**
INCC - May 1, 2008

Network Processors

- General Purpose Processors
- Control Plane Processors
- NPUs
- Custom IP
- FPGAs
- ASICS
- + Accelerators

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Summary

• General Purposes Processors were the early network processors

• Today’s networks are “intelligent” with very high bandwidth requiring significantly more packet processing

• Network Processors are multi-engine/core, multi-threaded SOCs with varying degree/ease of programmability and hardware acceleration

• Recent NPs are general-purpose coherent multi-processor, multi-threaded SOCs employing general purpose programming techniques