

CS 221 / CMPE 121: Digital Logic Design with Lab

Instructor: Dr Shahid Masud

Year: 2005-2006

Office No. & E-mail: 422, smasud@lums.edu.pk

Quarter: Winter

Office Hours: Mon, Tue, Wed 1130-1215 hrs

Category: Sophomore

Course Code: CS 221 / CMPE 121 **Course Title:** Digital Logic Design **Units:** 4

Course Description:

This is a core course in Computer Science as well as Computer Engineering programs. The course provides an introduction to basic principles and concepts of a digital system. The following topics are covered in detail: Number Systems, Boolean Algebra, Minimization Techniques, Combinational Logic Design, Sequential Circuits, Registers and Counters, Memory Systems and Parity circuits. This course acts as a foundation course to all other hardware and computer architecture courses.

Course Status:

Core course for Computer Science and Computer Engineering major

Pre-requisites:

None

Goals:

The goal of this course is to teach the foundations and concepts of Boolean algebra and digital logic design.

Text book:

“Digital Systems Principles and Applications” by Tocci and Widmer, Pearson Education, Eighth Edition

Supplementary Reading:

“Logic and Computer Design Fundamentals” by Morris Mano and Charles Kime, Prentice Hall Inc.

Lectures and Examinations:

- Two weekly lectures of 75 minutes duration each
- One weekly lab on Fridays in Electronics and Systems Lab
- Attendance is not compulsory, punctuality is desired
- One in-class midterm
- Comprehensive final examination

TA for the course:

To be announced on course website

Grading Scheme:

- Quizzes (6): 15%
- Eight Labs for 20%, marks breakup is as follows:
 - Attendance: 5%
 - Completion: 10%
 - Lab Exam: 5%
- Midterm: 30%
- Final: 35%

Lecture Topics:

Lecture No.	Course Topics	Readings
1	Introduction, Number Systems	Chap 1
2	Arithmetic Operations	Chap 2
3	BCD and Standard Codes, Parity Checkers	Chap 2
4	Logic Gates	Chap 2
5	Boolean Algebra	Chap 3
6	Boolean Simplification	Chap 3
7	Truth Tables and K-Maps	Chap 4
8	Minimization using K-Maps	Chap 4
9	Combinational Circuit Analysis and Design	Chap 4
10	Functions of Combinational Logic - Decoders	Chap 4
11	Digital Arithmetic: Adders and Subtractors	Chap 6
12	Code Converters, Multiplexers	Chap 9
	Midterm Exam	
14	Introduction to Latches and Flip-Flops	Chap 5
15	Types i.e. J-K, SR and D-Flip-Flops	Chap 5
16	Asynchronous and Synchronous Counters	Chap 5
17	Other Counters and Their Applications	Chap 7
18	Shift Registers	Chap 7
19	Shift Register Applications	Chap 7
20	Memory and Storage Devices	Chap 11

Lab Exercises:

Lab No.	Lab Topics
1.	Introduction to Lab and Experiments, Digital Logic Gate Operation (AND, OR, NAND, NOR, XOR)
2.	Basic Boolean Functions Implementation
3.	Decoders and Multiplexers
4.	Arithmetic Unit Design, Adders and Subtractors
5.	Study of NAND and NOR Latch
6.	Sequential Circuits: Analysis and Design
7.	Registers and Binary Counters
8.	Design Projects
9.	Completion of Outstanding tasks
10.	Final Lab Exam