1. SWITCHING FUNDAMENTALS

Switching is the provision of an on-demand connection between two end points. Two distinct switching techniques are employed in communication networks—circuit switching and packet switching.

Circuit switching provides a dedicated path between the two end points. The entire bandwidth of the connection is allocated for communication between the end points, for the duration of the call, whether or not messages are passed. In packet switching, on the other hand, messages to be passed are packetized and the connection is used by a call as and when packets are ready. In between these packets, the connection can be used to route packets belonging to other calls.

Circuit switching is ubiquitous in the telephone network. It is ideal for providing normal voice communications. It can also be used for data communications by employing modems which convert data to voice band signals.

Packet switching is popular in computer communication networks. Recently, however, it has started to proliferate into the telephone network under the asynchronous transfer mode (ATM) banner.

Need for Central Switching: When the number of stations N is small, we can simply interconnect the stations with a mesh network. When N gets larger, it is economical to use a central switch. When N is very large and the stations are spread over wide geographical area, one or more levels of intermediate switching is more economical. This leads to a hierarchical switching network, consisting of a network of switches. These scenarios are illustrated below.
**Four-Wire Switching:** The regular telephone instrument uses the same pair of wires for both transmitting (talking) and receiving (listening). This is known as *two-wire* transmission. This two-wire system, however, is converted to a *four-wire* system, which employs separate paths for each of the directions, to facilitate long distance transmission and switching. The device that performs this conversion is known as a "hybrid." Two separate paths have to be set up through the four wire switching matrix to complete a call as shown below.

![Four-Wire Switching Diagram](image)

2. **SPACE SWITCHING**

Space switching arrays are used in older analog as well as modern digital switching exchanges. They are also employed in the interconnection fabrics of fast packet switches. The techniques developed for the design and analysis of multistage space switches can be easily extended to the case of multistage time-space switching matrices.

**Single-stage space switch:** A single-stage space switch consists of a rectangular array of crosspoints. It can connect an arbitrary idle inlet to an arbitrary idle outlet. The space switch for connecting $N$ inlets to $N$ outlets requires $N^2$ crosspoints.

![An $n \times k$ space switch](image)

**Multistage space switching:** The number of crosspoints needed to build large single stage space switches grows as $N^2$. Furthermore, there is only one path from a specified inlet to a specified
outlet. This leads to a very inefficient utilization of the crosspoints and also raises reliability questions. Both of these problems can be solved by employing multistage switching matrices.

![Three-stage space switch](image)

The block diagram of a three-stage switch is shown in the diagram. In this structure the inlets and outlets are partitioned into subgroups of size \( n \) and there are \( k \) paths from an inlet to an outlet. The total number of crosspoints in such an implementation is given by:

\[
C = k \left( 2N + \frac{N^2}{n^2} \right)
\]

**Clo's Theorem for strictly nonblocking networks:** A strictly nonblocking network allows connection between an idle inlet-outlet pair, without disturbing existing connections, regardless of the previous state of the network. The requirements on a three-stage network that satisfies this condition can be derived as follows.

Suppose we want to set up a connection between an idle inlet \( a \) and an idle outlet \( b \) in a three-stage design. The worst scenario, as for as blocking is concerned, is shown in the diagram. All the \((n-1)\) inlets on the first stage switch originating inlet \( a \) and the \((n-1)\) outlets on the third stage switch terminating outlet \( b \) are busy. Furthermore, these \(2(n-1)\) connections are done via a different second stage switch. Under these circumstances, a further one second stage switch is required to connect \( a \) and \( b \). Thus, for a strictly nonblocking network, the minimum number of required second stage switches \( k = 2n-1 \). This is known as Clo's Theorem.

### 3. DIGITAL TIME DIVISION SWITCHING

**Time Slot Interchange (TSI) Module:** Suppose we want to build a 100 line strictly nonblocking telephone switch. This can be accomplished by a single stage or multistage space switch described previously. An alternate (and more economical) method is to use a time slot interchange (TSI) module. The architecture of such a switch is shown below:
In this method, channels are sampled at the standard 8 kHz rate (which yields a frame interval of 125 \( \mu s \)), coded at 8 bits per sample, and multiplexed to form a TDM signal. These channel samples are written sequentially into a 100 word data memory. The write address to this memory is generated by the time slot counter. The data memory is read in an order determined by the contents of a second 100 word memory known as the control memory. The output of the time slot counter serves as the read address of this control memory and its contents are programmed according to the required interconnection pattern between the inlets and outlets. As an example, to connect telephone lines 1 and 99, location 1 of the control memory is programmed with the number 99 and location 99 with the number 1, as shown in the diagram. When the contents of the data memory is read out using the output of the control memory as the read address, the output TDM line will have the proper time slots interchanged to realize the required connection. This TDM signal is demultiplexed, converted to analog, and directed to the proper telephone sets.

The combination of the data memory, time slot counter and the control memory is known as the TSI module (or a time switch). It can redirect a given input time slot to any desired output time slot. Hence, it is equivalent to a strictly nonblocking switch as shown below:

```
Inlet TDM Signal    Outlet TDM Signal
| N Time slots | TSI | N Time slots |
```

The TSI module described above employs a sequential write followed by a 'random' read to accomplish the switching function. It is known as an output controlled TSI module. Alternately, it is possible to realize the same function with an input controlled TSI module. In this case the control memory generates the write address of the data memory. The incoming voice samples are written into the appropriate locations of the data memory, depending on the desired switching function. The contents of the data memory are read out in a sequential order using the output of the time slot counter as the read address. The architecture of this TSI module is shown below:
**Channel limitations of the single stage time switch:** The data memory in the TSI module described above has to perform $N$ read operations and $N$ write operations during the frame interval of 125 $\mu$s, where $N$ denotes the number of channels in the TDM inlet/outlet signals. Assuming that a read or a write operation takes the same amount of time, equal to the memory cycle time, the maximum number of channels that can be switched with a single TSI module is given by:

$$\text{Maximum channels} = \frac{125 \, \mu s}{2 \times \text{memory cycle time in } \mu s}$$

As an example, we can switch 2500 channels with 25 ns memories.

**Increasing the capacity of the single stage time switch:** We will describe two methods for increasing the number of channels that can be switched with a single stage time switch.

The first method allows the capacity to be doubled. It uses two data memories in the **double buffering** mode as shown in the diagram. During odd numbered frames, data memory 1 is written into whereas data memory 2 is read. The roles are reversed in the even numbered frames. The TDM outlet is always connected to the output of the memory being read. As in the case of the normal TSI module, the control memory contains the desired interconnection pattern. This method requires twice the amount of data memory. The maximum switching delay can be close to two frames. The line rate of the TDM signals is also doubled.

The second method incorporates a technique of storing **multiple copies** of the input data. The number of copies stored equals the desired capacity increase over the normal TSI module. An architecture that doubles the capacity is shown in the diagram. The 2N input channels are multiplexed onto two TDM highways, labeled A and B, each consisting of N channels. The A channels are written into both the A1 and A2 data memories. Similarly, the B channels are written into both the B1 and B2 data memories. The channels appearing on the A TDM outlet are determined by the contents of control memory A. In each time slot, this memory outputs a read address which determines the data memory location to be read, and an output enable (OE) signal which determines whether memory A1 or B1 is to be enabled. This gives complete control over which one of the 2N channels appears in a particular time slot on the A TDM outlet. An identical method is used to determine the channels on the B TDM outlet.
Double Buffered TSI Module

Multiple Data Copy Method
4. MULTISTAGE TIME-SPACE SWITCHING

**Time-multiplexed space switch:** Multistage time-space architectures are necessary for the design of large switches. The time stages in these designs are similar to the TSI modules discussed previously. However, space switches that work in conjunction with time switches should be able to change their connection patterns on every time slot. Such space switches are known as *time multiplexed space switches* (TMSS). The architecture of an \( n \times k \) time multiplexed space switch operating on TDM signals which have \( N \) time slots is shown below:

A simple implementation of this switch consists of a bank of \( k \) selectors, each of which has the \( n \) TDM inlets, and an \( N \)-word control memory addressed by a time slot counter. The specific inlet selected by each of these selectors in every time slot is controlled by the output of the control memory. The number of bits required in the control word for this implementation is \( k \lceil \log_2 n \rceil \). Since this switch realizes a different interconnection pattern for each of the \( N \) time slots, its space equivalent representation consists of a bank of \( N \) \( n \times k \) switches, one for each time slot.

**Nonblocking STS Switch:** The TSI modules and the TMSS can be combined to implement large multistage networks. Consider the design of a \( nN \)-line switch using TSI modules capable of operating on TDM lines with \( N \) time slots. Such a switch can be implemented with an STS architecture shown below:

The equivalent space switch for the STS configuration is depicted below:
From Clo's theorem, we require \( k = 2n - 1 \) for this switch to be strictly nonblocking. It should be pointed out that, for a given total number of channels (\( nN \) in this case), we pick the value of \( N \) so as to operate the TSI modules close to their maximum speed. This usually leads to more economical designs since the cost of a memory bit is much smaller than that of a crosspoint. Assuming that a crosspoint costs \( M \) times as much as a memory bit, the complexity of the switch can be characterized by:

\[
\text{Switch complexity} = \text{Total amount of memory} + M \times \text{Total number of cross points}
\]

**Nonblocking TST switch:** To construct strictly nonblocking switches using the TST structure, we need TSI modules in which the number of time slots in the inlet TDM signal is different than that in the outlet TDM signal. Furthermore, we will set the first stage expansion ratio (or the third stage compression ratio) \( k/n = 2 \) to simplify the design. The design of TSI modules which perform the expansion and concentration functions is shown below:

It should be noted that the data and control memories in these TSI modules have to be twice as fast compared to the normal TSI module which has the same number of time slots on the inlets.
and outlets. Equivalently, for the same memory speed, the TDM signals terminating on the expander and concentrator TSI modules are allowed to contain only half as many channels.

The design of a strictly nonblocking TST switch using these modules and the TMSS is shown below for the case of $N = nk$ channels:

![TST Switch Diagram]

The space equivalent of this switch is:

![Space equivalent of TST switch Diagram]

The complexity of this switch can be evaluated as before.

Generally, for large strictly nonblocking switches, STS designs turn out to be more economical than TST designs. Furthermore, the delay through the STS switch is smaller.